

# NCV898031

## Small-Signal PSPICE Model

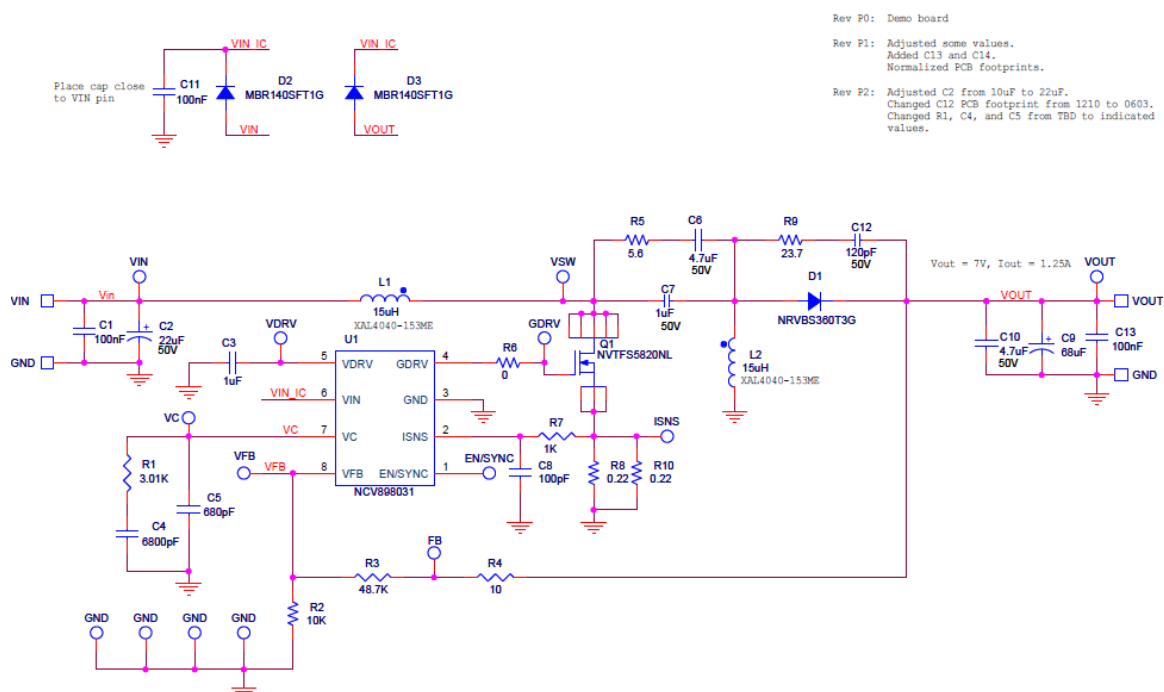
The NCV89803X-SMS model is a small-signal implementation of the 2 MHz non-synchronous SEPIC/Boost controller intended for AC analysis (cannot be used for large-signal transient analysis). The model is used for feedback loop stability analysis of an NCV898031 controller using a SEPIC topology.

The example PSPICE file demonstrates the model implementation used for the NCV898031SEPGEVB discrete inductor SEPIC evaluation demo board (Fig. 1).



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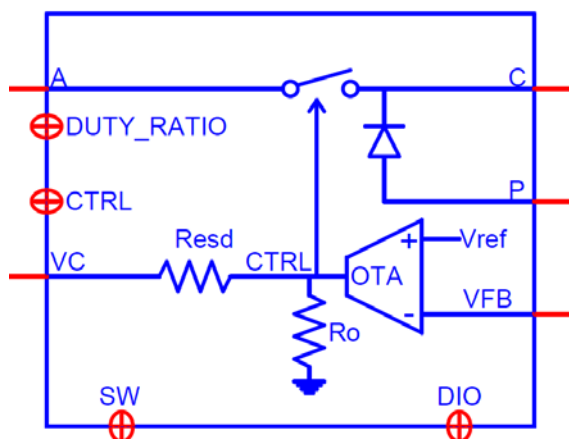


**Figure 1 NCV898031SEPGEVB Evaluation Board Schematic**

### Modeled Elements

This NCV89803X-SMS.LIB model is a modification of the public domain current-mode lossy switch PWMCM\_L.LIB model created by Christophe Basso [1]. The corresponding NCV89803X-SMS.OLB symbol representation is shown in Figure 2.

NCV898031-SMS  
 RI = 100m  
 L = 10u  
 U?  
 Value = NCV89803x-SMS



**Figure 2 NCV898031 Library Symbol**

The following elements have been added to the PWMCM\_L.LIB model to create the NCV89803X-SMS.LIB small-signal mode.

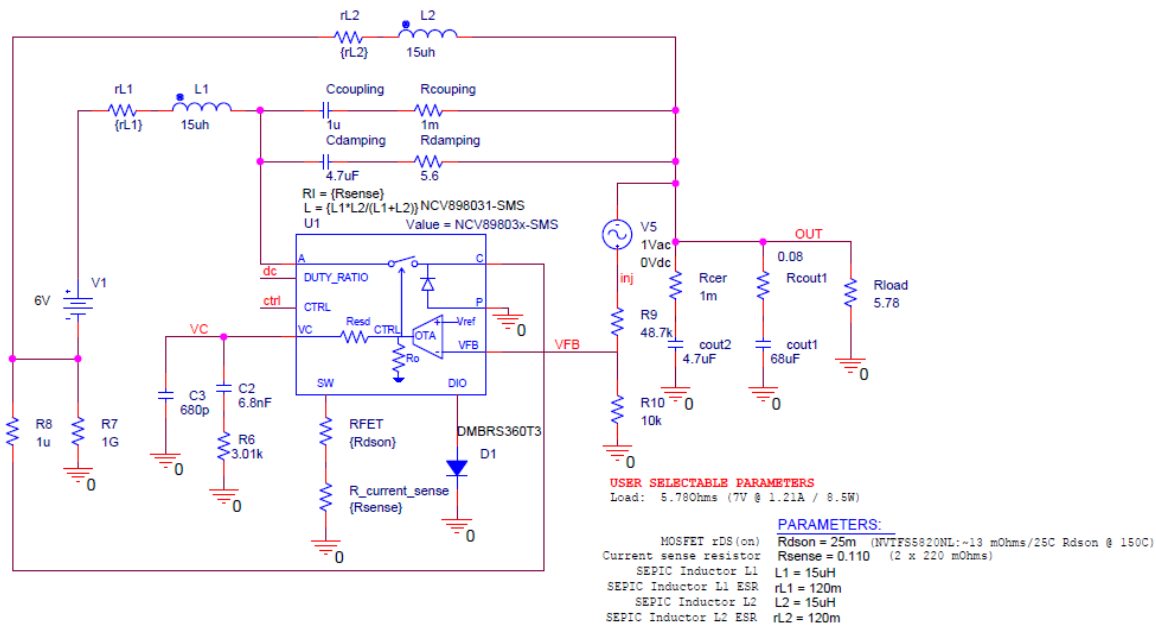
- The op amp characteristics
- IC specific controller slope compensation
- IC specific duty cycle limitation
- 2MHz oscillator frequency

A stability analysis of the SEPIC converter design may be performed by passing the following parameters to the NCV89803X-SMS model:

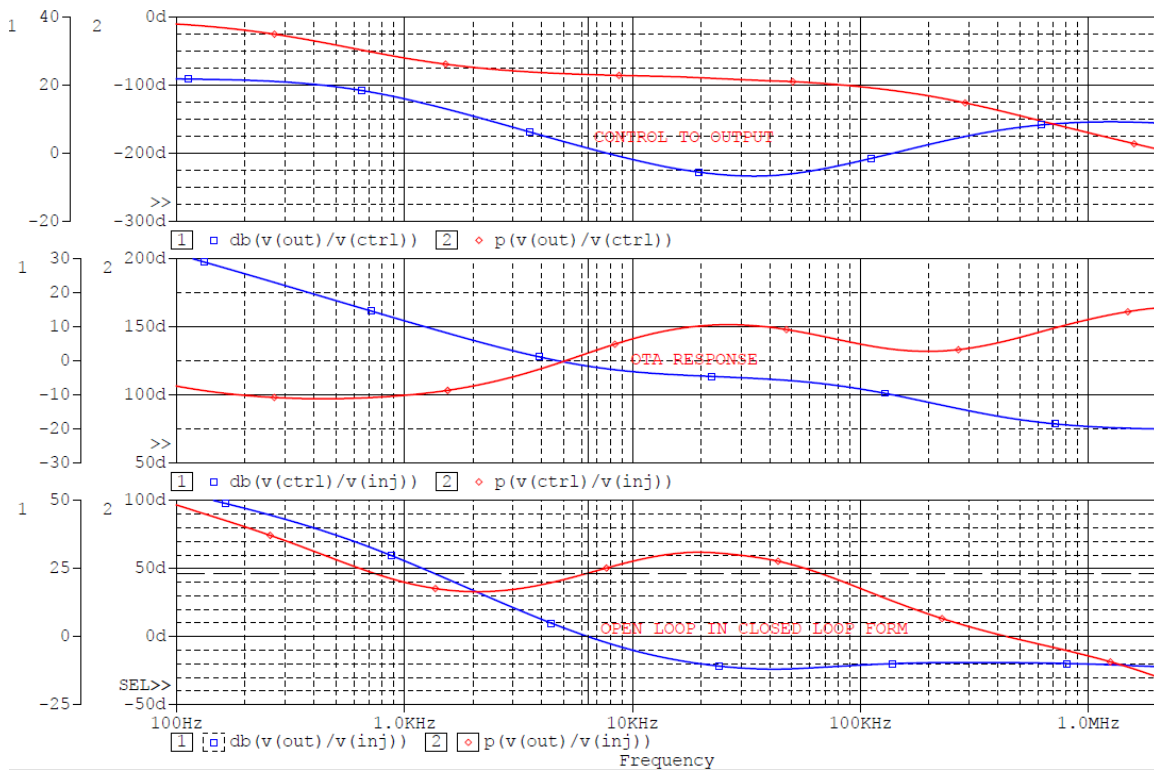
- SW: operating losses from the series combination of MOSFET  $r_{DS(ON)}$  and current sense resistor ( $\Omega$ )
- DIO – Connect the boost diode model for diode loss contribution. Anode to DIO and cathode to GND.
- L – Equivalent boost inductor (parallel combination of L1/L2 for SEPIC) (H)
- RI – Current sense resistor (value must be negative for boost topology) ( $\Omega$ )

## Modeling Example

A PSPICE small-signal analysis implementation of the NCV898031SEPGEVB demo board is shown in Fig. 3. Simulation results are shown in Fig. 4. Node definitions are provided in Table 1. The NCV898031 feedback amplifier is an operational transconductance amplifier (OTA). A  $542\ \Omega$  resistor between the OTA output and the IC-VC compensation pin is implemented in silicon for ESD protection. To permit an accurate OTA gain analysis when selecting compensation feedback components, the internal OTA output node (“CTRL”) is made available and strictly intended for analysis.



**Figure 3 NCV898031SEPGVB Evaluation Board Small-Signal Simulation**



An ESD protection resistor is present between the OTA output and the VC package pin on the die (this is not documented in the datasheet). A virtual output (CTRL) is provided to access the controller's internal feedback node to permit a more accurate analysis for instances where the compensation resistor approaches the value of Resd (set to 542Ω within the model).

**Table 1 NCV898031 Model – Node Definitions**

Parameter	Monitoring Purposes Only?	Unit	Range	Comment
A	No	V		Active Node (ref 1)
C	No	V		Common Node (ref 1)
P	No	V		Passive Node (ref 1)
DUTY_RATIO	Yes	N/A	0 – 0.83	INTERNAL NODE FOR SIMULATION ANALYSIS
CTRL	Yes	V	N/A	INTERNAL NODE FOR SIMULATION ANALYSIS
VC	No	V	N/A	IC Compensation Pin
VFB	No	V	$V_{ref} = 1.2\text{ V}$	Voltage feedback node
DIO	No	-	Boost Diode Loss	Connection point of boost diode's anode, only used for a more accurate duty ratio calculation in the simulation. Cathode MUST be connected to ground.
SW	No	-	rDS(on) and current sense losses	Connection point to include the influence of rDS(on) and current sense resistor losses, only used for a more accurate duty ratio calculation in the simulation.

**Table 2 NCV898031 Model – Parameters Table Definition**

Parameter	Unit	Comment
RI	$\Omega$	Current Sense Resistor
L	H	Boost Inductor

### Feedback Loop Analysis Methodology

Simulations should be run at worst case parameter conditions (e.g.: Minimum input voltage, worst case output capacitor parasitic ESR values, etc). Additional simulations under less stringent conditions (e.g. nominal ESR, different input voltage conditions) are recommended as well for verification. The disturbance injection point is introduced by inserting an AC source between nodes OUT and INJ.

#### 1- Control-Output (Modulator Plot) Response

This is the response of the power supply as seen by the IC's internal CTRL node ( $V(\text{OUT})/V(\text{CTRL})$ ). This information is required to select OTA compensation components (R6, C2, C3).

#### 2- OTA Compensation

From the modulator plot data, the OTA compensation network is determined ( $V(\text{CTRL})/V(\text{INJ})$ ) by selecting the desired zero gain and frequency values ( $R6/C2$ ) and pole frequency (C3). CTRL is the OTA output (before Resd) and is a node internal to the IC and is strictly intended for analysis.

#### 3- Loop Response (Open-Loop Response in Closed-Loop Form)

The power supply feedback loop response is obtained by plotting  $V(\text{OUT})/V(\text{INJ})$ . The resulting design cross-over frequency, phase-margin and gain-margin are now obtained.

### References

[1] C. Basso, "Switch-Mode Power Supplies – SPICE Simulations and Practical Designs", McGraw Hill, 2008.

[2] NCV898031: 2 MHz Non-Synchronous SEPIC / Boost Controller datasheet:

<http://onsemi.com/PowerSolutions/product.do?id=NCV898031>

[3] NCV898031: Automotive Grade High-Frequency SEPIC Controller Evaluation Board User's Manual:

[http://www.onsemi.com/pub\\_link/Collateral/EVBUM2167-D.PDF](http://www.onsemi.com/pub_link/Collateral/EVBUM2167-D.PDF)